APM32F103xE

Errata Sheet

Version: V 2.1

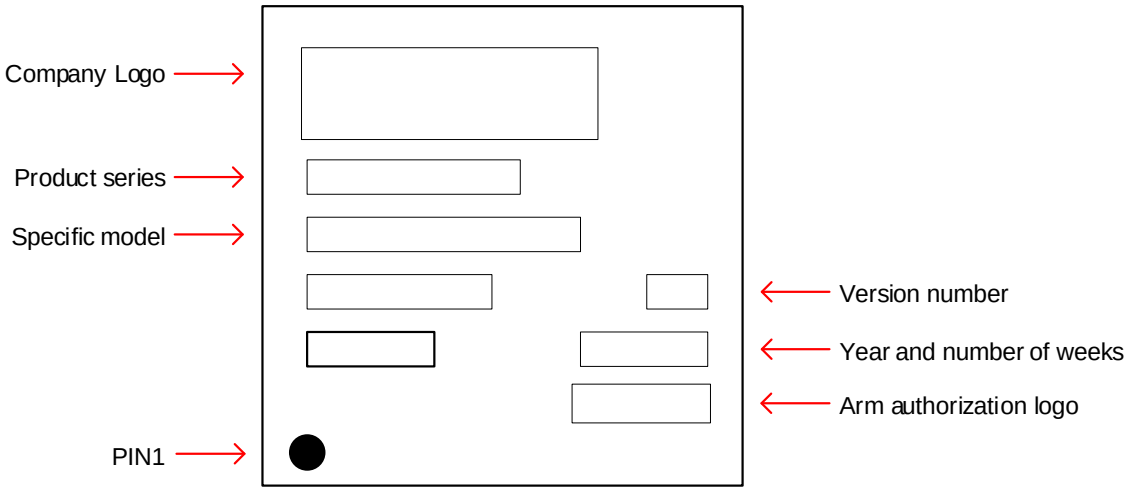
Contents

1 Introduction

This Manual mainly introduces the limitations of the APM32F103xE series products during use. If you encounter the application scenarios described in the manual during the use of the product, please use the product according to the solutions provided in the manual; if no solution is provided, please avoid this application scenario.

2 Product Version and Silk Screen Printing Instructions

Figure 1 Product Version and Silk Screen Printing Instructions



3 Errata List

Table 1 Errata List

Category	Introduction	Product version
		A1
GPIO	GPIO output	•
	PA12 cannot directly output the EVENTOUT signal of Arm® Cortex®-M3 core	•
	USART3 and FSMC remapping	•
Clock	HSE serves as the clock source	•
System	PWR sleep mode	•
	Float variable exception	•
	FPU functions	•
USBD/CAN	USBD interrupt	•
	Combined use of USBD/CAN	•
Flash	Low-power wake-up	•
	Flash erase	•

Note: "●" indicates that this errata description is involved in this version; the 'X' indicates that it is not involved in this version.

4 GPIO

4.1 GPIO output

Problem description

When the GPIO port is configured as multiplexing push-pull output, the output voltage may be affected by external interference and is unable to output accurate levels; when configured as floating input to read the external I/O input values, it may be affected by external interference and is unable to read accurate values.

Solutions

When configured as multiplexing push-pull output, connect an external pull-up resistor; when configured as floating input, connect an internal pull-up resistor externally or configure it as a pull-up input.

4.2 PA12 cannot directly output the EVENTOUT signal of Arm® Cortex®-M3 core

Problem description

PA12 cannot directly output the EVENTOUT pulse signal of Arm® Cortex®-M3 core.

Solutions

When PA12 outputs EVENTOUT pulse signal of Arm® Cortex®-M3 core, CAN_TX must be remapped first.

4.3 USART3 and FSMC remapping

Problem description

USART_USART3 remapping PD8 and PD9 pins conflicts with FSMC clock. Specifically: when remapping PD8 and PD9 as serial pins, enable FSMC clock but the serial communication cannot be used normally.

Solutions

Choose either of the following solutions:

- Use partial remapping function or default configuration of USART3.
- When USART3_TX is remapped to PD8 as a serial port pin, disable the SMC function.

5 Clock

5.1 HSE serves as the clock source

Problem description

When the timeout value of the software that sets the HSE startup time is too small (e.g. 0x0500), external clock startup ready timeout may occur, which may result in the failure of using HSE as the clock source.

Solutions

To ensure normal startup of the crystal oscillator, it is recommended to modify the external clock wait time timeout value to at least 0x3200.

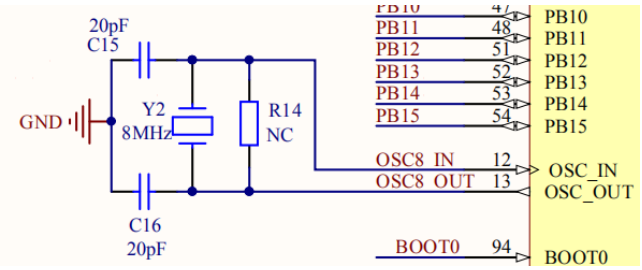
The specific operation is modifying the macro definition of HSE_STARTUP_TIMEOUT. Macro definition varies depending on the version of the library function:

- For the V3.x version library functions, the macro definition is in XXX32F10x.h;
- For the library before V3.0, the macro definition is in XXX32f10x_RCC.c.

The recommended crystal oscillator circuit is shown below (the capacitance value should match the crystal oscillator model)：

#define HSE_STARTUP_TIMEOUT ((uint16_t)0x3200) (recommended 0x3200, maximum 0xffff).

Figure 2 Crystal Oscillator Circuit



5.2 PLL frequency multiplication

Problem description

After doubling to 24MHz using PLL, the frequency output through the PA8 pin is unstable.

Solutions

Choose either of the following solutions:

- When using PLL multiplication, first use a large multiplication coefficient to increase the frequency of the VCO, and then output at a lower frequency. For example, increase the PLL frequency to 48MHz and then divide its frequency to 24MHz through an AHB prescaler.
- Related problems can be solved by migrating the E1 version.

6 System

6.1 PWR sleep mode

Problem description

The PWR sleep mode_WEF() instruction is invalid and cannot enter the low-power mode.

Solutions

Choose either of the following solutions:

- It can be executed normally after it is reset through the reset pin.
- Set in the download interface of Keil (set the reset and run)
- The second WFE instruction can be executed normally.
- Modify the program, and use 1 WFI rather than WFE.

6.2 Float variable exception

Problem description

Use the compilation project to add sc_math.lib to the engineering, and the program will crash when using a float variable.

Solutions

As long as sc_math.lib is added, the FPU clock must be enabled.

6.3 FPU functions

Problem description

The larger the input value of FPU is, the higher the probability of occurrence of errors is.

Solutions

Suggest controlling the FPU input value within ±3π. It is important to note that the operation acceleration effect of FPU only applies to the functions in the LIB library, and it has no significant acceleration effect on other operations such as +, -, ×, ÷, and matrix permutation.

7 USBD/CAN

7.1 USBD interrupt

Problem description

If the DM and DP data cables of USBD are both at high level, an abnormal interrupt will be caused and the operation of the main program will be affected. This is an unconventional operation.

Solutions

Choose either of the following solutions:

- Add the code suspended by FSUSP by force to the ESOF flag judgment of the USBD interrupt function.
- When starting the chip, first determine whether the I/O of D- is at a high or low level.
  - If it is at a high level, it indicates that it has been inserted into a charging device, and USBD initialization will be skipped, without enabling the USBD function;
  - If it is at a low level, it indicates that it has been inserted into a normal host, USBD is initialized normally, and USBD function is enabled.

7.2 Combined use of USBD/CAN

Problem description

APM32F103xE only has one CAN. USBD2 and CAN can be used simultaneously, USBD1 and CAN cannot be used simultaneously, and USBD1 and USBD2 cannot be used simultaneously.

Solutions

Use according to the recommendations of *Datasheet* and *User Manual*.

8 Flash

8.1 Low-power wake-up

Problem description

The low-power and AHB frequency division scenario may result in abnormal clearing of the dcode buffer, thus entering hardfault.

Solutions

For the WFI and WFE low-power wake-up scenarios:

- For the WFI low-power wake-up scenarios, AHB should not divide the frequency (i.e. ensure that the first interrupt vector data is read and returned from Flash, rather than returned from buf). After the low power is awakened, enter the interrupt service function, first read an address from each Flash bank in the interrupt service function and then start to execute the real user program.
- For the WFI low-power wake-up scenarios, AHB should not divide the frequency (i.e. ensure that the first interrupt vector data is read and returned from Flash, rather than returned from buf). After the low power is awakened, start sequential execution, first read an address from each bank and then start to execute the real user program.

8.2 Flash erase

Problem description

The erase operation and read Flash operation are performed concurrently, and a read Flash data error occurs when the erase operation is completed:

- The program executes FLASH ->SR status register in sequence, and read errors may occur.
- In the process of erasing Flash, an interrupt occurs, and the interrupt service function contains a program of reading data from Flash, and data errors may occur when erasing is completed, and thus causes program exceptions.

Solutions

Choose either of the following solutions:

- For regular erase scenarios (program sequential execution), after initiating erase, before executing FlASH_GetBank1Status, add:
  while (FLASH->SR&FLASH_FLAG_BANK1_BSY)==FLASH_FLAG_BSY;
  And AHB keeps the frequency not divided.
- For regular erase scenarios (program sequential execution), after the state is read for the first time, it will be executed once again before the total state returns:
  FLASH_GetBank1Status sub-function
  And AHB keeps the frequency not divided.

- For the interrupt scenarios, before erasing Flash, shield the interrupt, there will be no scenarios of entering the interrupt in the erasing process, and it will change to the regular erase scenario.
- For the interrupt scenarios, add a statement of waiting for the Flash erase operation to end at the beginning of the interrupt service function:
  while (FLASH->SR&FLASH_FLAG_BANK1_BSY)==FLASH_FLAG_BSY;
  Wait for the Flash erase operation to end, then execute the interrupt service program, and keep the AHB frequency not divided.

9 Revision history

Table2 Document Revision History

Date	Version	Revision History
August 2024	1.0	New edition
August 2025	2.1	(1) Add Chapter5.2

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